

***IN THE UNITED STATES PATENT AND TRADEMARK OFFICE***

<b>APPLICANTS:</b>	Hammond <i>et al.</i>	<b>CONF. NO.:</b>	2980
<b>SERIAL NUMBER:</b>	10/797,231	<b>ART UNIT:</b>	2812
<b>FILING DATE:</b>	March 10, 2004	<b>EXAMINER:</b>	Ghyka, Alexander G.
<b>TITLE:</b>	METHOD OF SELECTIVE REMOVAL OF SIGE ALLOYS		

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**COMMENTS ACCOMPANYING PRE-APPEAL BRIEF REQUEST FOR REVIEW**

This paper is submitted along with a Pre-Appeal Brief Request for Review in accordance with the Official Gazette Notice dated July 12, 2005, and a Notice of Appeal in response to the final Office action mailed by the U.S. Patent and Trademark Office on May 15, 2007. The Director is hereby authorized to charge the required fee of \$500 for the Notice of Appeal to Deposit Account No. 07-1700. Applicants believe that no additional fee is required for this submission to be entered. However, please consider this a conditional petition for the proper extension, if one is required, and a conditional authorization to charge any related extension fee, or any other fees, necessary for entry of this submission to Deposit Account No. 07-1700.

Applicants' **Remarks** begin on page 2 of this paper.

## REMARKS

The Examiner has failed to consider an essential element of independent claims 28 and 46 in rejecting those claims and claims dependent therefrom under 35 U.S.C. § 102(b) over K. Ismail, "Si/SiGe High-Speed Field Effect Transistors," IEEE IEDM Tech. Dig., pp. 509-512, 1995 ("Ismail"). We therefore submit that the rejection is improper and that review is appropriate pursuant to the Official Gazette Notice dated July 12, 2005.

In particular, independent claims 28 and 46 recite a method including the step of "selectively removing said SiGe layer to expose said strained semiconductor layer." The Examiner contends that Ismail teaches such a method, but flatly ignores the fact that Ismail is utterly silent about the specific process steps utilized to achieve his structure of Figure 7. Ismail states no more than the fact that both strained Si and strained SiGe layers are epitaxially grown on Si substrates. *See* Ismail, p. 510, right column, bottom paragraph. The Examiner contends that the mere fact that both channels are grown, along with the fact that "the two top layers of the stack between the P-MODFET and N-MODFET are narrower than the layers below on the N-MODFET side" indicate that a portion has been selectively removed. However, the Examiner ignores the fact that Ismail's Figure 7 structure could be constructed in ways not involving selective removal. For example, the layers on the P-MODFET side and in the middle of the structure could be selectively added to the base structure present on the N-MODFET side. Such a technique would still involve both strained channels being epitaxially grown, and would account for the specific geometry of the top two layers in Figure 7. This fact, along with Ismail's utter silence on selective removal of any kind, clearly renders Ismail a non-anticipatory reference with respect to independent claims 28 and 46 and claims dependent therefrom.

Moreover, the Examiner has failed to consider another essential feature of independent claim 46 in rejecting that claim and claims dependent therefrom under 35 U.S.C. § 102(b) over Ismail. Namely, independent claim 46 recites "providing a gate dielectric over said strained semiconductor layer." The Examiner ignores the fact that Ismail's Figure 7 structure utilizes Schottky (i.e., metal) gates, "which are known to have higher leakage current than insulated gates." *See* Ismail, p. 511, left column, first paragraph (emphasis added). While Ismail's Figure 9 structure does incorporate an SiO<sub>2</sub> gate dielectric, this structure is planar, lacking even the

**CONCLUSION**

We respectfully submit that, as set forth in the foregoing remarks, there are clear errors in the Examiner's rejections.

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Respectfully submitted,



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